CLAIMS

1. A memory storage device comprising:

a storage medium having a plurality of coverage areas, each of said coverage areas having a storage area associated therewith, each of said storage areas being configurable in one of a plurality of structural states to represent information stored in said storage area;

a plurality of electron beam emitters configured to electrically communicate with said storage medium, said storage medium and said plurality of emitters being configured to move relative to each other such that each of said emitters is capable of providing a beam of electrons to a respective one of said coverage areas of said storage medium;

a first current source configured to selectively electrically communicate with at least one of said plurality of electron beam emitters so as to enable the at least one of said emitters to provide a beam of electrons to a respective one of said coverage areas; and

a control system electrically communicating with said first current source, said control system configured to facilitate a controlled current flow from said first current source to the at least one of said emitters.

2. The memory storage device of claim 1, wherein the at least one of said emitters is a field emitter.

3. The memory storage device of claim 1, wherein said control system comprises:

a first current mirror electrically communicating with said first current source and the at least one of said emitters, said first current mirror having a first stage and a second stage, said first stage electrically communicating with said second stage, said first stage being configured to receive current from said first current source and provided current to said second stage, said second stage being configured to receive current from said first stage and to enable a controlled current to be provided to the at least one of said emitters, said controlled current corresponding to a predetermined current to be provided to the at least one of said emitters.

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4. The memory storage device of claim 3, wherein said control system comprises:

a switch electrically communicating with said second stage, said switch being configured to selectively provide said controlled current to the at least one of said emitters.

5. The memory storage device of claim 3, wherein said control system comprises:

means for selectively providing said controlled current to the at least one of said emitters.

6. The memory storage device of claim 3, wherein said first stage has a first transistor and said second stage has a second transistor, said first transistor having a gate, a source, and a drain, said second transistor having a gate, a source, and a drain, said gate and said drain of said first transistor electrically communicating with said first current source and said gate of said second transistor, said source of said first transistor and said source of said second transistor being provided to ground.

7. The memory storage device of claim 3, wherein said control system comprises:

a second current source configured to selectively electrically communicate with the at least one of said emitters; and

a second current mirror electrically communicating with said second current source and the at least one of said emitters, said second current mirror having a first stage and a second stage, said first stage electrically communicating with said second stage, said first stage being configured to receive current from said second current source and provided current to said second stage, said second stage being configured to receive current from said first stage and enable a controlled current to be provided to the at least one of said emitters, said controlled current corresponding to a predetermined current to be provided to the at least one of said emitters, wherein said control system is configured to selectively provided to the at least one of said emitters one of only said controlled current corresponding to said first current source, a summation of said controlled current corresponding to said first current source and said controlled current corresponding to said second current source, and no current.

8. The memory storage device of claim 3, wherein each stage of said first current mirror has multiple transistors.

9. The memory storage device of claim 4, wherein said control system comprises:

a controller electrically communicating with said switch, said controller being configured to enable said switch to selectively provide said controlled current to the at least one of said emitters.

10. The memory storage device of claim 4, wherein said switch is a transistor.

11. The memory storage device of claim 6, wherein said first transistor and said second transistor are field effect transistors.

12. The memory storage device of claim 7, wherein said controller comprises:

logic configured to selectively provide only said controlled current corresponding to said first current source to the at least one of said emitters so as to facilitate reading of information from said storage medium; and

logic configured to selectively provide a summation of said controlled current corresponding to said first current source and said controlled current corresponding to said second current source to the at least one of said emitters so as to facilitate writing information to said storage medium.

13. The memory storage device of claim 9, wherein said controller comprises:

logic configured to enable said switch to selectively provide said controlled current to the at least one of said emitters

14. The memory storage device of claim 13, wherein said logic is embodied on a computer-readable medium.

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15. A method for providing current to an emitter of a memory storage device, the memory storage device having a storage medium and a plurality of electron beam emitters configured to electrically communicate with the storage medium, the storage medium and the plurality of emitters being configured to move relative to each other such that each emitter may provide a beam of electrons within a respective coverage area of the storage medium, each coverage area having a storage area formed therein being configurable in one of a plurality of structural states to represent information stored in the storage area, said method comprising:

providing a first current source and a first current mirror electrically communicating with the first current source;

controlling a current flow from the first current source to at least one of the emitters by:

providing current from the first current source to the first current mirror; and

selectively providing current from the first current mirror to the at least one of the emitters.

16. The method of claim 15, wherein the step of selectively providing current from the first current mirror to the at least one of the emitters comprises the step of:

electrically interposing a switch between the first current mirror and the at least one of the emitters such that the switch enables the current provided from the first current mirror to be selectively provided to the at least one of the emitters.

17. The method of claim 15, further comprising the steps of:

providing a second current source and a second current mirror electrically communicating with the second current source;

controlling a current flow from the second current source to at least one of the emitters by:

providing current from the second current source to the second current mirror; and

selectively providing current from the second current mirror to the at least one of the emitters.

18. The method of claim 17, further comprising the steps of:

selectively providing only current corresponding to the first current source to the at least one of the emitters so as to facilitate reading of information from the storage medium; and

selectively providing a summation of current corresponding to the first current source and current corresponding to the second current source to the at least one of the emitters so as to facilitate writing information to the storage medium.

19. The method of claim 18, wherein the step of selectively providing a summation of current comprises the step of:

providing a switch electrically interposed between the second current mirror and the at least one of the emitters such that the switch enables current corresponding to the second current source to be summed with current corresponding to the first current source.

20. The method of claim 19, wherein the step of selectively providing a summation of current comprises the step of:

providing a controller electrically communicating with the switch, the controller being configured to provide at least one control signal to the switch such that, in response to the at least one control signal, the switch enables current corresponding to the second current source to be summed with current corresponding to the first current source.

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